MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to a manufacturing method of a CSP (Chip Size Package) type semiconductor device.

Description of the Related Art:

The CSP receives attention in recent years as a three-dimensional mounting technology as well as a new packaging technology. The CSP means a small package having about the same outside dimensions as those of a semiconductor die packaged in it.

A BGA type semiconductor device has been known as a type of CSP. A plurality of ball-shaped conductive terminals made of metal such as solder is arrayed in a grid pattern on one principal surface of a package of the BGA type semiconductor device and is electrically connected with the semiconductor die mounted on the other side of the package.

When the BGA type semiconductor device is mounted on electronic equipment, the semiconductor die is electrically connected with an external circuit on a printed circuit board by compression bonding of each of the conductive terminals to each of wiring patterns on the printed circuit board.

Such a BGA type semiconductor device has advantages in providing a large number of conductive terminals and in size reduction over other CSP type semiconductor devices such as an SOP (Small Outline Package) and a QFP (Quad Flat Package), which have lead pins protruding from their sides. The BGA type semiconductor device is used as an image sensor chip for a digital camera incorporated into a mobile telephone, for example.

Figs. 9A and 9B show an outline structure of a conventional BGA type semiconductor device. Fig. 9A is an oblique perspective figure showing a top side of the BGA type semiconductor device. And Fig. 9B is an oblique perspective figure showing a back side of the BGA type semiconductor device.

A semiconductor die 101 is sealed between a first glass substrate 104a and a second glass substrate 104b through epoxy resins 105a and 105b in the BGA type semiconductor device 100. A plurality of ball-shaped conductive terminals (hereafter referred to as conductive terminals) 111 is arrayed in a grid pattern on a principal surface of the second glass substrate 104b, that is, on a back surface of the BGA type semiconductor device 100. The conductive terminals 111

are connected to the semiconductor die 101 through a plurality of second wirings 109. The plurality of second wirings 109 is connected with first wirings pulled out from inside of the semiconductor die 101, making each of the conductive terminals 111 electrically connected with the semiconductor die 101.

More detailed explanation on a cross-sectional structure of the BGA type semiconductor device 100 is given hereafter referring to Fig. 10. Fig. 10 shows a cross-sectional view of the BGA type semiconductor devices 100 divided along dicing lines into individual dice.

The first wiring 103 is provided on an insulation film 102 on a top surface of the semiconductor die 101. The semiconductor die 101 is bonded to the first glass substrate 104a with the resin 105a. A back surface of the semiconductor die 101 is bonded to the second glass substrate 104b with the resin 105b. One end of the first wiring 103 is connected to the second wiring 109. The second wiring 109 extends from the end of the first wiring 103 to a surface of the second glass substrate 104b. The ball-shaped conductive terminal 111 is formed on the second wiring 109 extended onto the second glass substrate 104b.

SUMMARY OF THE INVENTION

The invention provides a method of manufacturing a semiconductor device. The method includes bonding a supporting substrate to a first surface of a semiconductor wafer on which a semiconductor element is formed, and back-grinding a second surface of the semiconductor wafer. The second surface is opposite to the first surface. The method also includes reducing a roughness of the back-ground second surface by etching the back-ground second surface.

The invention provide another method of manufacturing a semiconductor device. The method includes bonding a supporting substrate to a first surface of a semiconductor wafer on which a semiconductor element is formed, and forming a groove in the semiconductor wafer by etching a second surface of the semiconductor wafer. The second surface is opposite to the first surface. The method also includes rounding a corner of the groove by etching the second surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view showing a manufacturing method of a semiconductor device according an embodiment of this invention.

Fig. 2 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Fig. 3 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Fig. 4 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Fig. 5 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Fig. 6 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Fig. 7 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Fig. 8 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

Figs. 9A and 9B are oblique perspective views showing a manufacturing method of a semiconductor device according to a conventional art.

Fig. 10 is a cross-sectional view showing the manufacturing method of the semiconductor device according to the conventional art.

DETAILED DESCRIPTION OF THE INVENTION

First some of the problems that this invention is directed to will be explained. As shown in FIGS. 9A-10, the glass substrates are bonded to both surfaces of the semiconductor die 101 in the BGA type semiconductor device 100 described above. However, it is not necessarily required that the second glass substrate 104b is bonded to the surface on which no semiconductor element is formed, in other words, the surface over which the conductive terminals are disposed. That is to say, there is no need for bonding the second glass substrate as long as the second wiring 109 is insulated from the semiconductor die 101. When the glass substrates are bonded to both surfaces of the semiconductor die, thickness of the two glass substrates makes up most of total thickness of the semiconductor device 100. Thus, the glass substrate is bonded only to the surface of the semiconductor die 101 on which a semiconductor element is formed, so that cost and size of the semiconductor device 100 are reduced. An example of such a semiconductor device will be described using Fig. 8 which is a cross-sectional view of the semiconductor device according to this invention. The semiconductor device similar to the semiconductor device 100 is made by forming an insulation film 7 on the semiconductor die 1 instead of bonding the

second glass substrate, and forming a cushioning pad 8, a second wiring 9, a protection film 10 and a conductive terminal 11 over the insulation film 7. However, there are problems to be described bellow in making such semiconductor device.

First, in manufacturing the BGA type semiconductor device, the surface opposite to the surface to which a glass substrate 4 is bonded, that is, a back surface of the semiconductor device is ground by back-grinding, prior to forming the insulation film 7. A semiconductor wafer, in which a plurality of the semiconductor dice is included, is ground with a whetstone in the back-grinding. The back-grinding transfers bumps and dips on the whetstone to the surface of the wafer and causes scratches extending several microns in depth and length. The back-grinding scarcely causes a problem in the case of the semiconductor device 100 shown in Fig. 10, since the bumps and dips on the surface of the wafer due to the scratches are covered by the resin 105b.

However, in the case of the BGA type semiconductor device having the glass substrate only on the surface on which the semiconductor element is formed, like in the case of the semiconductor device of this embodiment, it is required that an insulation film 7 is formed on the back-ground surface of the wafer in order to provide insulation between the die and the second wiring. Because the insulation film 7 is formed with a CVD (Chemical Vapor Deposition) apparatus, the bumps and dips on the surface of the wafer are transferred to the insulation film 7 and the surface of the insulation film 7 is formed uneven. This causes poor coverage of photoresist films used in patterning the insulation film 7 and the second wiring 9. The poor coverage of the photoresist film used in patterning the insulation film 7 may cause pinholes or cracks, making a contributing factor to deteriorate yield and reliability of the semiconductor device.

Next problem is as follows. After the back-grinding, grooves are formed by etching the semiconductor wafer along border lines in order to divide the semiconductor wafer into individual semiconductor dice. Residues and foreign particles attached to the etched surface of the semiconductor wafer cause bumps and dips on the surface of the semiconductor wafer. Also sharp edges are left at corners of the grooves after the etching. As a result, coverage of photoresist films for patterning, the second wiring 9 and the protection film 10 to be formed after forming the grooves is degraded, making additional factors to deteriorate yield and reliability of the semiconductor device.

This invention is directed to solve the problems addressed above, and offers a method to resolve the problems due to the bumps and dips on the surface of the back-ground semiconductor wafer, the bumps and dips on the surface of the etched semiconductor wafer and the sharp edges at the corners left after forming the grooves.

A manufacturing method of a semiconductor device according to an embodiment of this invention will be described referring to Figs. 1 through 8.

A semiconductor wafer 1a, which will form semiconductor dice 1 in later process steps, is provided as shown in Fig. 1. The semiconductor dice 1 are CCD image sensor chips, for example, and are manufactured by a semiconductor wafer processing. A pair of first wirings 3 separated by a predetermined spacing is formed on a first surface of the semiconductor wafer through an insulation film 2 near a border (referred to as a dicing line or a scribe line) S for dividing the wafer 1a into individual semiconductor dice 1. Each of the pair of first wirings 3 makes a pad extended from a bonding pad in the semiconductor die 1 to proximity of the border S. That is, each of the pair of first wirings 3 is a pad for external connection, and is electrically connected with a circuit in the semiconductor die 1, which is not shown in the figure.

Then a supporting plate is bonded with an adhesive to the first surface of the semiconductor wafer 1a on which the first wirings 3 are formed. A transparent epoxy resin 5 is used as the adhesive and a transparent glass substrate 4 is used as the supporting plate in this embodiment. When the BGA type semiconductor device of this invention is manufactured to house an LSI such as a memory or a microcomputer and does not house the CCD, an opaque plastic supporting plate may be bonded using a suitable adhesive.

A second surface of the semiconductor wafer 1a opposite to the first surface to which the glass substrate 4 is bonded is back-ground to reduce a thickness of the wafer, as shown in Fig. 2. The thickness of the back-ground wafer is about 230 μm.

On the back-ground second surface of the semiconductor wafer 1a, scratches are formed to produce bumps and dips extending several microns in width and depth, as shown in an encircled portion a (a surface before etching) in Fig. 2. The second surface of the semiconductor wafer 1a is wet-etched using a chemical solution having high selection ratio between an etch rate of silicon (hereafter referred to as Si) which is a material forming the semiconductor wafer 1a and an etch rate of silicon dioxide (hereafter referred to as SiO_2) which is a material forming the glass substrate 4. The semiconductor wafer 1a is reduced in thickness by 5 to 30 μm by the

wet-etching to obtain a surface with reduced bumps and dips, as shown in an encircled portion b (a surface after etching) in Fig. 2.

Any etching solution may be used in the wet-etching, as long as it has high selection ratio between the etch rate of Si and the etch rate of SiO_2. For example, a mixed solution composed of 2.5% of hydrofluoric acid, 50% of nitric acid, 10% of acetic acid and 37.5% of water is used as the wet-etching solution in this embodiment.

Either of methods described below may be used as the wet-etching method.

A first method is to reduce the bumps and dips on the second surface by wet-etching which includes dripping the chemical solution on the semiconductor wafer 1a with the glass substrate 4 bonded to it while holding the wafer so that the back-ground second surface of the semiconductor wafer 1a faces upward and spreading the chemical solution all over the second surface of the semiconductor wafer 1a by spinning the semiconductor wafer 1a around its center. This is similar to spin coating of a resist material.

In this method, the roughness on the second surface is further reduced by reversing direction of rotation of the semiconductor wafer 1a to spread the chemical solution more equally all over the second surface of the semiconductor wafer 1a.

A second method is to reduce the roughness on the second surface by wet-etching performed by dipping the semiconductor wafer 1a into the chemical solution. The roughness on the second surface is more uniformly reduced by the second method than by the first method described above, because the chemical solution pervades all the second surface of the semiconductor wafer 1a more uniformly by the second method thean the first method.

A third method is to reduce the roughness on the back-ground second surface of the semiconductor wafer 1a by CMP (Chemical Mechanical Polishing).

Instead of the wet-etching, the roughness on the second surface of the semiconductor wafer 1a may be reduced by dry-etching the back-ground second surface of the semiconductor wafer while holding it upward.

After the wet-etching, a photoresist film (not shown in the figure) which has an opening along the border S is formed on the second surface of the semiconductor wafer 1a opposite to the first surface to which the glass substrate 4 is bonded, as shown in Fig. 3. Isotropic etching of the semiconductor wafer 1a using the photoresist film as a mask forms a tapered groove along the border S to expose the insulation film 2. Although the semiconductor wafer 1a is divided

into individual dice 1 by the isotropic etching, the semiconductor dice 1 are held together with the glass substrate 4, keeping the separated dice 1 together as one unit.

Note that the isotropic etching may be performed by either dry-etching or wet-etching.

Bumps and dips as well as residues and foreign particles from the etching are left on the second surface of the semiconductor wafer 1a after forming the groove. In addition, the semiconductor dice have sharp edges at corners of the groove as shown in circles denoted as c and d in Fig. 3.

Wet-etching is performed to reduce the residues and the foreign particles and round the sharp edges as shown in Fig. 4. The sharp edges shown in portions c and d in Fig. 3 are rounded off as shown in portions c and d in Fig. 4.

Chemical solution similar to one used in the wet-etching after the back-grinding may be used in the wet-etching after forming the groove. Following methods are applicable to the wet-etching after forming the groove.

A first method of wet-etching after forming the groove is dripping the chemical solution on the semiconductor wafer 1a while holding the surface with the groove upward and spreading the chemical solution all over the surface with the groove of the semiconductor wafer 1a by spinning the semiconductor wafer 1a.

In this method, uniformity of the etching over the surface with the groove is improved by reversing direction of rotation of the semiconductor wafer 1a to spread the chemical solution more equally all over the surface with the groove of the semiconductor wafer 1a.

A second method of the wet-etching after forming the groove is dipping the semiconductor wafer 1a into the chemical solution. The uniformity of etching over the surface with the groove is improved by the second method, because the chemical solution pervades the entire surface with the groove of the semiconductor wafer 1a more uniformly by the dipping than the wet-etching by the first method described above.

Instead of the wet-etching, dry-etching may be applied to the surface with the groove of the semiconductor wafer 1a after forming the groove to round the sharp edges at the corners of the groove.

After the wet-etching, the insulation film 7 is formed on the surface of the semiconductor wafer 1a opposite to the surface to which the glass substrate 4 is bonded, as shown in Fig. 5. A silane-based oxide film of 3 μm in thickness is formed in this embodiment.

A photoresist film (not shown) is applied on the insulation film 7 and patterning in the insulation film 7 is made to expose a portion of a bottom surface of each of the first wirings 3, as shown in Fig. 6. That is, the insulation film 7 and the insulation film 2 are etched off using the photoresist film as a mask to expose the portion of the bottom surface of each of the first wirings 3. Next, flexible cushioning pads 8 are formed at locations above which the conductive terminals 11 are to be formed. The cushioning pads 8 have function to absorb power applied through the conductive terminals 11 and relax stress when the conductive terminals 11 are bonded. However this embodiment does not necessarily require the cushioning pads 8.

Then the second wiring 9 is formed on the surface opposite to the surface to which the glass substrate 4 is bonded. The first wirings 3 are electrically connected with the second wiring 9.

A photoresist film (not shown) is applied on the surface opposite to the surface to which the glass substrate 4 is bonded and pattering is made to form an opening in the photoresist film along the border S, as shown in Fig. 7. Etching is performed using the photoresist film as a mask to remove a portion of the second wiring 9 along the border S. After patterning the second wiring 9, electroless plating is made on the surface opposite to the surface to which the glass substrate 4 is bonded so that Ni-Au plating (not shown) is applied on the second wirings 9.

Then the protection film 10 is formed on the surface opposite to the surface to which the glass substrate 4 is bonded. In order to form the protection film 10, the surface opposite to the surface to which the glass substrate 4 is bonded is held upward, a thermosetting organic resin is dropped on it and the organic resin is spread over the surface by spinning the semiconductor wafer 1a utilizing centrifugal force. The protection film 10 is formed on a surface of the second wirings 9.

Portions of the protection film 10 at locations where the conductive terminals 11 are to be formed (i.e. locations on the cushioning pads 8) are removed by etching using a photoresist film (not shown) as a mask, as shown in Fig. 8. Then the conductive terminals 11 are formed on the second wirings 9 at the locations exposed by the etching (locations corresponding to the cushioning pads 8). Finally, the protection film 10, the resin 5 and the glass substrate 4 are cut along the border S to complete the BGA type semiconductor device.

The embodiment described above is directed to the BGA type semiconductor device having the ball-shaped conductive terminals 11. However, this embodiment is not limited to the

BGA type semiconductor device and may be applied to a semiconductor device which does not have the ball-shaped conductive terminals such as an LGA (Land Grid Array) type semiconductor device, for example.

With this invention, the problems in manufacturing the CSP type semiconductor device are solved and yield, and reliability of the CSP type semiconductor device are improved.